Appl. No. 10/817,207
Reply Filed: April 12, 2007
Reply to Final Office Action of: October 12, 2006

REMARKS

In response to the Final Office Action of October 12, 2006, the Applicants submit this Reply. In view of the foregoing amendments and following remarks, reconsideration is requested.

Claims 1-3 remain in this application, of which claim 1 is independent. No fee is due for claims for this amendment.

Rejections Under 35 U.S.C. §102

Claims 1-6, of which claims 1 and 4 are independent, were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,613,162 ("Kabenjian"). In view of the cancellation of claims 4-6, without prejudice, the rejection is moot. As for claims 1-3, the rejection is respectfully traversed.

According to Kabenjian, during initiation, the CPU 100: writes a destination address, size of the transfer and other control data to the DMA controller 202; requests control of the memory bus 110; executes one or more read/write cycles addressed to the IDE device 156; initializes the DMA unit 200; writes to source, destination and count registers A; and writes go and direction data to the command register. See Kabenjian, col. 10, lines 5-61. After setting up the register set A 300 for a first DMA transfer, the CPU 100 either resets the first DMA channel for a second DMA transfer (col. 10, ll. 62-64), or uses a two-deep shadowing technique of "writing appropriate values to register set B of the first register block while the DMA unit is performing the previously initialized DMA transfer" (col. 11, ll. 3-6) or uses multiplexing to quickly switch between register set A or B. (col. 11, ll. 19-21).

In contrast, in claim 1, the DMA controller, not the CPU, *loads the stored parameters* (addressing, counters, pointers to buffer control units, etc.) that enable the data access between the port and the memory.

Claim 1 recites (with emphasis added) "wherein the *direct memory access controller stores parameters* defining the direct memory access operations for each port, and wherein after a request is received from a port *the direct memory access controller loads the parameters for a direct memory access operation* responsive to the request from the port to enable the port to access the memory and transfer data between the memory and the buffer associated with the port."

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The Final Office Action also noted that the claims did not require that the FIFO's be connected to the devices, in other wods, being on the device's side. In view of this comment, the claims have been amended to clarity that the buffer in question is "located at and is dedicated to" the port. Support for this language is found in Fig. 1 of this application. Thus, the claims as amended further distinguish the invention from Kabenjian.

Accordingly, in view of the foregoing amendments and remarks, claim 1 is distinguishing from Kabenjian. Dependent claims 2 and 3 are allowable for at least the same reasons.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this reply, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, please charge any fee to **Deposit Account No. 50-0876.**

Respectfully submitted,

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